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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,566	06/29/2001	Jun-Cheng Ko	LAM2P258	6944

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,566	KO ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 16-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/16/2004 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tao (US 5,871,658) in view of Winniczek et al (US 6,228,278)

Tao discloses a method for monitoring and controlling a plasma etch method for forming a patterned layer. This method comprises the steps of:

forming a transistor structure on a surface of a substrate 50 (col 9, lines 44-46)

forming an interlevel dielectric layer 60 on/directly over the surface of the substrate 50 (fig. 5), as seen in fig. 5, there is no etch stop layer formed on the substrate

plasma etching a contact hole/opening though the dielectric layer 60 in a RIE etch chamber (col 6, lines 55-57; col 10, lines 40-55)

monitoring a DC bias of the plasma etcher/plasma processing chamber during etching (col 7, lines 29-31, fig. 3)

using a plasma controller and an OES detector to control the bias voltage (col 7, lines 26-31), the OES detects the endpoint of an etching step (col 2, lines 35-37)

Unlike the instant claimed invention as per claims 1, 21, Tao does not specifically disclose the step of discontinuing the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

However, Winniczek discloses a method for determining an etch endpoint comprises the step of discontinuing the plasma etch upon detecting an endpoint signaling change in the bias compensation voltage change/increasing compensation voltage applied to an ESC (col 3, lines 1-7; col 4, lines 1-3, col 6, lines 16-20)

Since Tao discloses using a plasma controller and an OES detector to control the bias voltage, one skilled in the art would have found it obvious to modify Tao method by discontinuing the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage as per Winniczek because Winniczek states that his inventive endpoint technique is highly sensitive and is capable of accurately providing endpoint information even when etching substrates having a small fraction of the layer exposed to the etching plasma (col 7, lines 34-38)

Regarding claims 2, 21, fig. 6 of Tao shows that the surface of the substrate 50 is exposed at the end of the etching step.

The limitations of claims 3, 5, 22, 23 have been discussed above.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tao (US 5,871,658) in view of Winniczek et al (US 6,228,278) and further in view of Ko (US 5,854,135)

Tao as modified by Winniczek has been described above. Regarding claim 4, Tao also discloses forming source/drain regions 58a and 58b along the gate structure (col 9, lines 47-50). Unlike the instant claimed invention as per claim 4, Tao and Winniczek fail to disclose the step of forming spacers along sidewall of the gate structure.

Ko discloses a dry etching method comprises the step of forming spacers along sidewall of the gate structure (col 4, lines 35-37, fig. 1)

Hence, one skilled in the art would have found it obvious to modify Tao and Winniczek by adding the step of forming spacers along sidewall of the gate structure to form insulator spacers as taught by Ko (col 4, lines 36-37)

5. Claims 6-8, 10 are rejected under 35 U.S.C.103(a) as being unpatentable over Ko (US 5,854,135) in view of Winniczek et al (US 6,228,278)

Ko discloses a method of creating a small diameter SAC opening by dry etching. This method comprises the steps of:

forming a transistor structure on a substrate 1, the transistor structure includes a gate structure formed over a surface of the substrate (fig. 1)

forming spacers 8 along sidewall of the gate structure (col 4, lines 36-37)

forming source/drain region into the surface of the substrate, the source/drain regions 9 are formed outside of the spacers 8 along sidewall of the gate structure (col 4, lines 43-45, fig. 2)

forming an interlevel dielectric layer 10a on/directly over the first surface of the substrate (col 4, lines 65-67; fig. 2), as seen in fig. 2, there is no etch stop layer formed on the substrate

forming a contact hole and a via hole 12 and 13 through the dielectric layer 10a using a plasma etching step (col 5, lines 40-50; fig. 5), as seen in fig. 5, the contact hole and a via hole 12 and 13 define a top layer of the gate structure 50 and source/drain regions 9

determining endpoint using the opening/via formed during the etching step (col 5, lines 44-47)

Unlike the instant claimed invention as per claim 6, Ko does not specifically disclose the step of monitoring an ESC bias compensation voltage during the plasma etching and discontinuing the plasma etch upon detecting a endpoint signaling change in the ESC bias compensation voltage.

However, Winniczek discloses a method for determining an etch endpoint comprises the step of monitoring an ESC bias compensation voltage during the plasma etching and discontinuing the plasma etch upon detecting an endpoint signaling change in the bias compensation voltage change/increasing compensation voltage applied to an ESC (col 3, lines 1-7; col 4, lines 1-3, col 6, lines 16-20)

Since both Ko and Winniczek are concerned with a step of detecting an endpoint of a plasma etching step, one skilled in the art would have found it obvious to modify Ko

method by monitoring an ESC bias compensation voltage during the plasma etching and discontinuing the plasma etch upon detecting a endpoint signaling change in the ESC bias compensation voltage as per Winniczek because Winniczek states that his inventive endpoint technique is highly sensitive and is capable of accurately providing endpoint information even when etching substrates having a small fraction of the layer exposed to the etching plasma (col 7, lines 34-38)

Regarding claim 7, fig. 5 of Ko shows that the portion of top layer of the gate structure and a portion of the source/drain are exposed at the end of the etching step.

Regarding claim 8, Ko discloses forming a gate oxide 3 (col 3, lines 65-66) and polysilicon gate 4 (col 4, lines 25-26)

Regarding claim 10, KO discloses the step of forming a silicon oxide layer and etching the silicon oxide layer to form spacers 8 (col 4, lines 31-37)

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ko (US 5,854,135) in view of Winniczek et al (US 6,228,278) and further in view of Liaw (US 5,843,815)

Ko as modified by Winniczek has been described above in paragraph 5. Unlike the instant claimed invention as per claim 9, Ko and Winniczek do not disclose depositing an oxide layer over the first surface of the substrate, the gate structure and spacer, depositing a TEOS layer over the oxide and an oxide layer over the TEOS.

However, Liaw discloses a process for forming a MOSFET device/transistor comprises the steps of depositing an oxide layer 10 over the first surface of the

substrate, the gate structure and spacer, depositing a TEOS layer 30 over the oxide and an oxide layer 19 over the TEOS (col 4, lines 17-18, col 5, lines 10-24, fig. 7)

Hence, one skilled in the art would have found it obvious to modify Ko and Winniczek by forming an insulating composite structure as per Liaw because according to Liaw a composite interlevel dielectric resulting in a smooth topology (col 5, lines 21-32)

7. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tao (US 5,871,658) in view of Winniczek et al (US 6,228,278)

Tao discloses a method for monitoring and controlling a plasma etch method for forming a patterned layer. This method comprises the steps of:

forming a transistor structure on a surface of a substrate 50 (col 9, lines 44-46)

forming an interlevel dielectric layer 60 on/directly over the surface of the substrate 50 (fig. 5), as seen in fig. 5, there is no etch stop layer formed on the substrate

placing the substrate into a chamber (fig. 3), plasma etching a contact hole/opening though the dielectric layer 60 in a RIE etch chamber (col 6, lines 55-57; col 10, lines 40-55)

introducing etchant gas into the chamber (col 8, lines 9-12)

applying power to the chamber to start the plasma etching process (col 9, lines 3-7)

monitoring a DC bias of the plasma etcher/plasma processing chamber during etching (col 7, lines 29-31, fig. 3)

using a plasma controller and an OES detector to control the bias voltage (col 7, lines 26-31), the OES detects the endpoint of an etching step (col 2, lines 35-37)

Unlike the instant claimed invention as per claim 16, Tao does not specifically disclose the step of discontinuing the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

However, Winniczek discloses a method for determining an etch endpoint comprises the step of discontinuing the plasma etch upon detecting an endpoint signaling change in the bias compensation voltage change/increasing compensation voltage applied to an ESC (col 3, lines 1-7; col 4, lines 1-3, col 6, lines 16-20)

Since Tao discloses using a plasma controller and an OES detector to control the bias voltage, one skilled in the art would have found it obvious to modify Tao method by discontinuing the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage as per Winniczek because Winniczek states that his inventive endpoint technique is highly sensitive and is capable of accurately providing endpoint information even when etching substrates having a small fraction of the layer exposed to the etching plasma (col 7, lines 34-38)

Regarding claims 17, fig. 6 of Tao shows that the surface of the substrate 50 is exposed at the end of the etching step.

The limitations of claims 18, 20, 24 have been discussed above.

Response to Arguments

8. Applicant's arguments with respect to claims 1-10, 16-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
February 12, 2004